REMARKS

Claims 1-30 were pending in this application.

Claims 1-22 have been rejected.

Claims 23-30 were previously withdrawn and have been cancelled.

Claims 1-22 have been amended as shown above.

Claims 1-22 remain pending in this application.

Reconsideration and full allowance of Claims 1-22 are respectfully requested.

I. ALLOWABLE CLAIMS

The Applicants thank the Examiner for the indication that Claims 4, 9, 14, 18, and 21 would be allowable if rewritten in independent form to include the elements of their respective base claims and any intervening claims and to overcome a rejection under 35 U.S.C. § 112. Because the Applicants believe that the remaining claims in this application are patentable, the Applicants have not rewritten Claims 4, 9, 14, 18, and 21 in independent form.

II. OBJECTIONS TO THE SPECIFICATION

The Office Action objects to the Abstract as failing to describe the claimed invention. The Applicants have amended the Abstract. The Applicants respectfully submit that the Abstract as amended describes the claimed invention. The Applicants respectfully request withdrawal of the objection to the specification.

III. REJECTION UNDER 35 U.S.C. § 112

The Office Action rejects Claims 3-9, 13-18, 21, and 22 under 35 U.S.C. § 112, second paragraph, as failing to particularly point out and distinctly claim the subject matter regarded as the invention.

Regarding Claims 3 and 13, the Office Action asserts that it is unclear how a "vertical plug" is mounted on a "metal pad" when various layers of material are disposed on the "metal pad." (*Office Action, Page 4, First paragraph*). The Applicants have amended Claims 3 and 13 to recite that the "vertical plug" is mounted in "electrical connection with" or is "electrically connected to" the "metal pad" and that an "undoped silicon oxide layer" is deposited on a "portion of the metal pad." These amendments resolve the ambiguity noted in the Office Action. The Office Action also asserts that it is unclear how a "redistribution metal layer" is electrically connected to the "vertical plug" if the vertical plug is covered by the layers of material. (*Office Action, Page 4, First paragraph*). The Applicants respectfully note Claims 3 and 13 do not require that the layers of material cover the "vertical plug." Even if the layers of material cover the "vertical plug," the vertical plug could be exposed through etching or other mechanism. Based on this, the Applicants respectfully submit that Claims 3 and 13 are definite.

Regarding Claims 5 and 15, the Office Action asserts that it is unclear how a "redistribution metal layer" is electrically connected to a "metal pad" when layers of material are disposed on the "metal pad." (*Office Action, Page 4, Second paragraph*). The Applicants have amended Claims 5 and 15 to recite that an "undoped silicon oxide layer" is deposited on "at least a portion of the metal pad" and that a "metal layer" is in "electrical connection with" or is

"electrically connected to" the "metal pad." The Applicants respectfully note that the "metal layer" may be in "electrical connection with" or "electrically connected to" the "metal pad" in any suitable manner. For example, the layers of material (such as the "undoped silicon oxide layer") may be deposited only on a portion of the "metal pad," and the "metal layer" may be deposited directly on another portion of the "metal pad." As another example, the layers of material (such as the "undoped silicon oxide layer") may be deposited on the entire "metal pad," and the "metal layer" may be deposited in "electrical connection with" or "electrically connected to" the "metal pad" through vias or other openings etched in the layers of material. Based on this, the Applicants respectfully submit that Claims 5 and 15 are definite.

Regarding Claims 7 and 17, the Office Action asserts that it is unclear how a layer of silicon oxynitride is deposited over all portions of a "metal redistribution layer" when a layer of silicon oxynitride has already been deposited over all portions of the "metal redistribution layer" (as recited in the "last step" of Claims 5 and 15). (*Office Action, Page 4, Third paragraph*). The Applicants have amended Claims 5 and 15 to recite that a "silicon oxynitride layer" is deposited over "at least some portions" of a metal layer. The Applicants have also amended Claims 7 and 17 to recite that the "silicon oxynitride layer" is deposited over "all portions of the metal layer." Based on this, the Applicants respectfully submit that Claims 7 and 17 are definite.

For these reasons, the Applicants submit that Claims 3, 5, 7, 13, 15, and 17 (and their dependent claims) are definite and comply with 35 U.S.C. § 112. Accordingly, the Applicants respectfully request withdrawal of the § 112 rejection of Claims 3-9, 13-18, 21, and 22.

IV. REJECTION UNDER 35 U.S.C. § 102

The Office Action rejects Claims 1, 2, 10-12, 19, and 20 under 35 U.S.C. § 102(a) as being anticipated by "Applicant Admitted Prior Art" ("*AAPA*"). The Office Action rejects Claims 1-3, 5-8, 10-13, 15-17, 19, 20, and 22 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,441,467 to Toyosawa et al. ("*Toyosawa*"). The Applicants respectfully traverse these rejections.

A prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. (*MPEP § 2131; In re Bond, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990)*). Anticipation is only shown where each and every limitation of the claimed invention is found in a single prior art reference. (*MPEP § 2131; In re Donohue, 766 F.2d 531, 534, 226 U.S.P.Q. 619, 621 (Fed. Cir. 1985)*).

AAPA illustrates a portion of an integrated circuit chip (element 100). (*Application, Page 2, Lines 15-16*). The integrated circuit chip is fabricated by first manufacturing a silicon layer (element 160), active circuits (element 170), a metal pad (element 150), and a passivation layer (element 180). (*Application, Page 3, Lines 11-17*). This completes fabrication of the "basic functional chip." (*Application, Page 3, Lines 18-19*). After that, a redistribution metal layer (element 140), a secondary passivation layer (element 190), and an under bump metallurgy (UBM) layer (element 130) are fabricated. (*Application, Page 3, Lines 19-21*).

AAPA clearly recites that the "basic functional chip" (including the "active circuits") are fabricated in one stage, and the "redistribution metal layer" is fabricated during a separate stage.

AAPA lacks any mention of fabricating the "redistribution metal layer" during at least part of the fabrication of the "basic functional chip." As a result, *AAPA* fails to anticipate "fabricating a portion of [an] integrated circuit" that includes "at least one active circuit area" and "fabricating a redistribution metal layer at least partially during fabrication of the portion of the integrated circuit" as recited in Claim 1. *AAPA* also fails to anticipate an integrated circuit that includes a "portion comprising at least one active circuit area" and a "redistribution metal layer fabricated at least partially during fabrication of the portion of the integrated circuit" as recited in Claim 11.

For these reasons, *AAPA* fails to anticipate the Applicants' invention as recited in Claims 1 and 11 (and their dependent claims).

Toyosawa recites a semiconductor device that includes an "active element" (element 20) and a "metal layer" (element 14). (*Col. 6, Lines 34-35; Col. 6, Line 66 – Col. 7, Line 3*). The Office Action asserts that the active element (element 20) of *Toyosawa* anticipates the "active circuit area" recited in Claims 1 and 11. (*Office Action, Page 5, Section 12, Second paragraph*). The Office Action also asserts that the metal layer (element 14) of *Toyosawa* anticipates the "redistribution metal layer" recited in Claims 1 and 11. (*Office Action, Page 5, Section 12, Second paragraph*).

Claims 1 and 11 recite that the "redistribution metal layer" is fabricated "at least partially during fabrication" of a portion of an integrated circuit, where the portion includes "at least one active circuit area." Based on these recitations, in order to show that *Toyosawa* anticipates Claims 1 and 11, the Office Action must establish that *Toyosawa* fabricates the metal layer (element 14) at least partially during fabrication of the active element (element 20). The Office

Action cannot make this showing.

Toyosawa contains absolutely no mention that fabrication of the metal layer (element 14) at least partially overlaps with fabrication of the active element (element 20). In fact, *Toyosawa* recites just the opposite – fabrication of the active element (element 20) is complete before fabrication of the metal layer (element 14) begins. The active element (element 20) of *Toyosawa* represents a combination of components (elements 1-9). (*Col. 6, Lines 20-35*). Figures 4(a) through 4(c) of *Toyosawa* illustrate how the components of the active element (element 20) are fabricated first. (*Col. 7, Line 63 – Col. 8, Line 13*). Figures 4(d) through 4(f) illustrate how additional layers (including the metal layer 14) are fabricated after fabrication of the active element (element 20) is complete. (*Col. 8, Lines 14-40*).

Based on this, *Toyosawa* clearly fails to anticipate fabricating a redistribution metal layer "at least partially during fabrication" of a portion of an integrated circuit that includes an "active circuit area" as recited in Claims 1 and 11. For these reasons, *Toyosawa* fails to anticipate the Applicants' invention as recited in Claims 1 and 11 (and their dependent claims).

Accordingly, the Applicants respectfully request withdrawal of the § 102 rejections and full allowance of Claims 1-3, 5-8, 10-13, 15-17, 19, 20, and 22.

V. CONCLUSION

As a result of the foregoing, the Applicants assert that the claims in this application are in condition for allowance and respectfully request an early allowance of such claims.

SUMMARY

If any outstanding issues remain, or if the Examiner has any further suggestions for expediting allowance of this application, the Applicants respectfully invite the Examiner to contact the undersigned at the telephone number indicated below or at *wmunck@davismunck.com*.

The Commissioner is hereby authorized to charge any additional fees connected with this communication (including any extension of time fees) or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,
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Date: June 30, 2004

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